CLAIMS

1. A method comprising:

splitting an optical stream into a primary optical stream and a secondary optical stream;

converting the secondary optical stream to an electrical signal;

processing the electrical signal to identify a particular portion of the optical stream;

delaying the primary optical stream to provide a delayed optical stream; and

modifying the particular portion of the delayed optical signal.

2. The method of claim 1 wherein said processing comprises:

recovering a clock signal and a data signal from the electrical signal; and

identifying the particular portion based on at least one of the clock signal and the data signal.

3. The method of claim 1 further comprising:

generating a gating signal at the particular position based on said processing; and

wherein said modifying the particular portion is based on the gating signal.

4. The method of claim 1 wherein said modifying the particular portion comprises inverting at least one bit in the particular portion of the delayed optical stream.

5. The method of claim 1 wherein said modifying the particular portion comprises suppressing at least one bit in the particular portion of the delayed optical stream.

6. The method of claim 1 wherein said particular portion comprises a particular bit position in the optical stream.

7. The method of claim 1 wherein the optical stream comprises a SMPTE-standard video stream.

8. The method of claim 1 wherein the optical stream comprises a SMPTE259M video stream.

9. The method of claim 8 wherein said modifying the particular portion of the delayed optical signal introduces at least one bit error in the SMPTE259M video stream.

10. The method of claim 9 wherein said processing the electrical signal to identify a particular portion of the optical stream comprises identifying at least one of an active video portion, a horizontal ancillary data portion, a vertical ancillary data portion, a start active video timing portion and an end active video timing portion of the SMPTE259M video stream.

11. An apparatus comprising:

an optical splitter to split an optical stream into a primary optical stream and a secondary optical stream;

an optoelectronic converter to convert the secondary optical stream to an electrical signal;

a processor to process the electrical signal to identify a particular portion of the optical stream;

an optical delay to delay the primary optical stream to provide a delayed optical stream; and

an optical switch responsive to the processor to modify the particular portion of the delayed optical signal.

12. The apparatus of claim 11 wherein the processor comprises:

a phase-locked loop/clock recovery component to recover a clock signal and a data signal from the electrical signal; and

a logic component to identify the particular portion based on at least one of the clock signal and the data signal.

13. The apparatus of claim 11 wherein the processor is to generate a gating signal at the particular position based on said processing, and wherein the optical switch is to modify the particular portion based on the gating signal.

14. The apparatus of claim 11 wherein the optical switch is to modify the particular portion by inverting at least one bit in the particular portion of the delayed optical stream.

15. The apparatus of claim 11 wherein the optical switch is to modify the particular portion by suppressing at least one bit in the particular portion of the delayed optical stream.

16. The apparatus of claim 11 wherein said particular portion comprises a particular bit position in the optical stream.

17. The apparatus of claim 11 wherein the optical stream comprises a SMPTE-standard video stream.

18. The apparatus of claim 11 wherein the optical stream comprises a SMPTE259M video stream.

19. The apparatus of claim 18 wherein the optical switch is modify the particular portion of the delayed optical signal to introduce at least one bit error in the SMPTE259M video stream.

20. The apparatus of claim 19 wherein the processor is to identify at least one of an active video portion, a horizontal ancillary data portion, a vertical ancillary data portion, a start active video timing portion and an end active video timing portion of the SMPTE259M video stream.

21. A method comprising:

identifying a particular portion of an in-transit SMPTE-standard digital video stream, the particular portion selected from the group consisting of an active video portion, a horizontal ancillary data portion, a vertical ancillary data portion, a start active video timing portion and an end active video timing portion; and

introducing at least one bit error in the particular portion of the in-transit SMPTE-standard digital video stream.

22. The method of claim 21 wherein the in-transit SMPTE-standard digital video stream comprises an in-transit SMPTE259M digital video stream.

23. The method of claim 21 further comprising:

decoding the in-transit SMPTE-standard digital video stream having the at least one bit error to produce a plurality of video frames; and

examining an effect of the at least one bit error on at least one of the video frames.

24. The method of claim 21 wherein the in-transit SMPTE-standard digital video stream is embodied by an optical signal.

25. The method of claim 21 wherein the in-transit SMPTE-standard digital video stream is embodied by an electrical signal.

26. An apparatus comprising:

a processor to identify a particular portion of an in-transit SMPTE-standard digital video stream, the particular portion selected from the group consisting of an active video portion, a horizontal ancillary data portion, a vertical ancillary data portion, a start active video timing portion and an end active video timing portion; and

a switch responsive to the processor to introduce at least one bit error in the particular portion of the in-transit SMPTE-standard digital video stream.

27. The apparatus of claim 26 wherein the in-transit SMPTE-standard digital video stream comprises an in-transit SMPTE259M digital video stream.

28. The apparatus of claim 26 further comprising:

a decoder to decode the in-transit SMPTE-standard digital video stream having the at least one bit error to produce a plurality of video frames.

29. An apparatus comprising:

a logic component to identify a particular portion of an in-transit SMPTE-standard digital video stream, the particular portion selected from the group consisting of an active video portion, a horizontal ancillary data portion, a vertical ancillary data portion, a start active video timing portion and an end active video timing portion, and to introduce at least one bit error in the particular portion of the in-transit SMPTE-standard digital video stream.

30. The apparatus of claim 29 wherein the in-transit SMPTE-standard digital video stream comprises an in-transit SMPTE259M digital video stream.

31. The apparatus of claim 29 further comprising:

a decoder to decode the in-transit SMPTE-standard digital video stream having the at least one bit error to produce a plurality of video frames.